

METHOD AND APPARATUS FOR ADJUSTING TIMING
IN A DIGITAL SYSTEM

ABSTRACT OF THE DISCLOSURE

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A method and apparatus for adjusting timing in a digital system or telecommunication system includes processing that begins by dividing a data clock by a 1st value to produce a divided data clock. The processing continues by dividing an analog front-end clock by a 2nd value to produce a divided analog front-end clock. The 1st and 2nd values are selected such that the divided data clock and the divided analog front-end clock have similar clock rates. The processing continues by comparing the phase of the divided data clock with the phase of the divided analog front-end clock to produce a phase difference. The processing continues by adjusting the analog front-end clock based on the phase difference to produce an adjusted analog front-end clock.

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